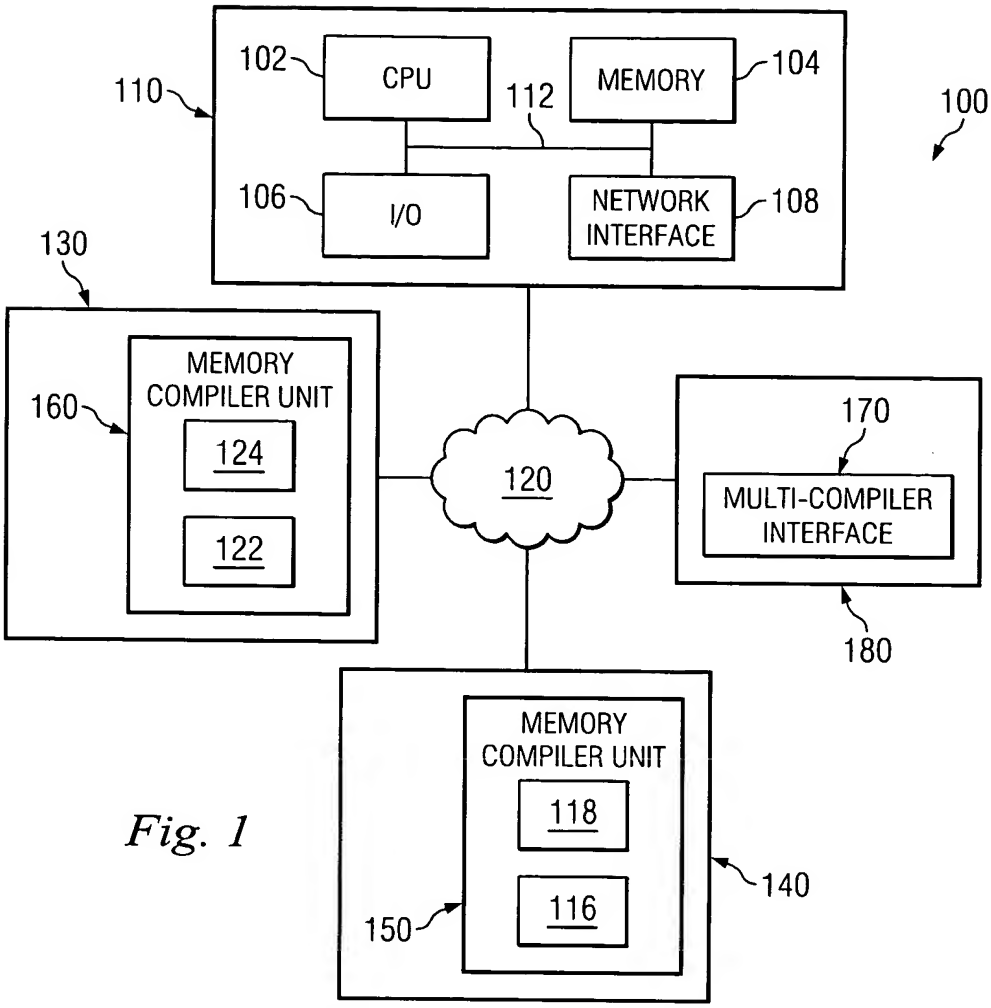

102
CPU
MEMORY
104
110
112
100
106
I/O
NETWORK INTERFACE
108
130
MEMORY COMPILER UNIT
160
124
122
120
170
MULTI-COMPILER INTERFACE
180
MEMORY COMPILER UNIT
118
116
150
140

Fig. 1

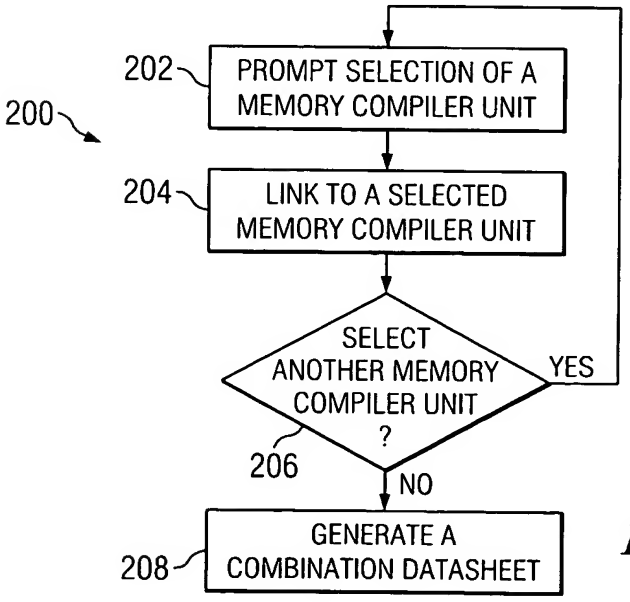
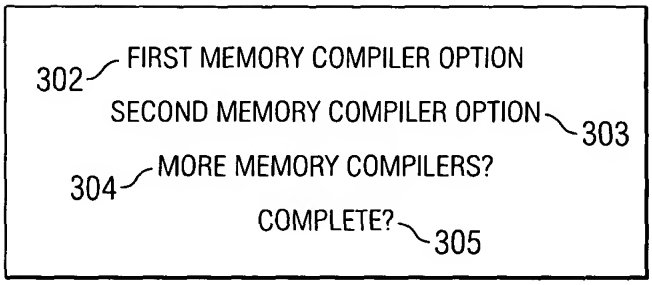

202
PROMPT SELECTION OF A MEMORY COMPILER UNIT
200
204
LINK TO A SELECTED MEMORY COMPILER UNIT
SELECT ANOTHER MEMORY COMPILER UNIT ?
YES
206
NO
208
GENERATE A COMBINATION DATASHEET

Fig. 2

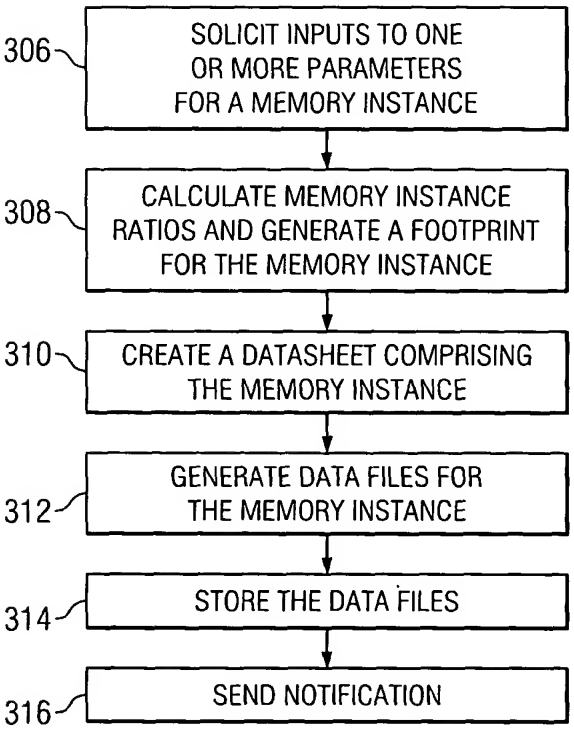
300a

Fig. 3a



300b

Fig. 3b



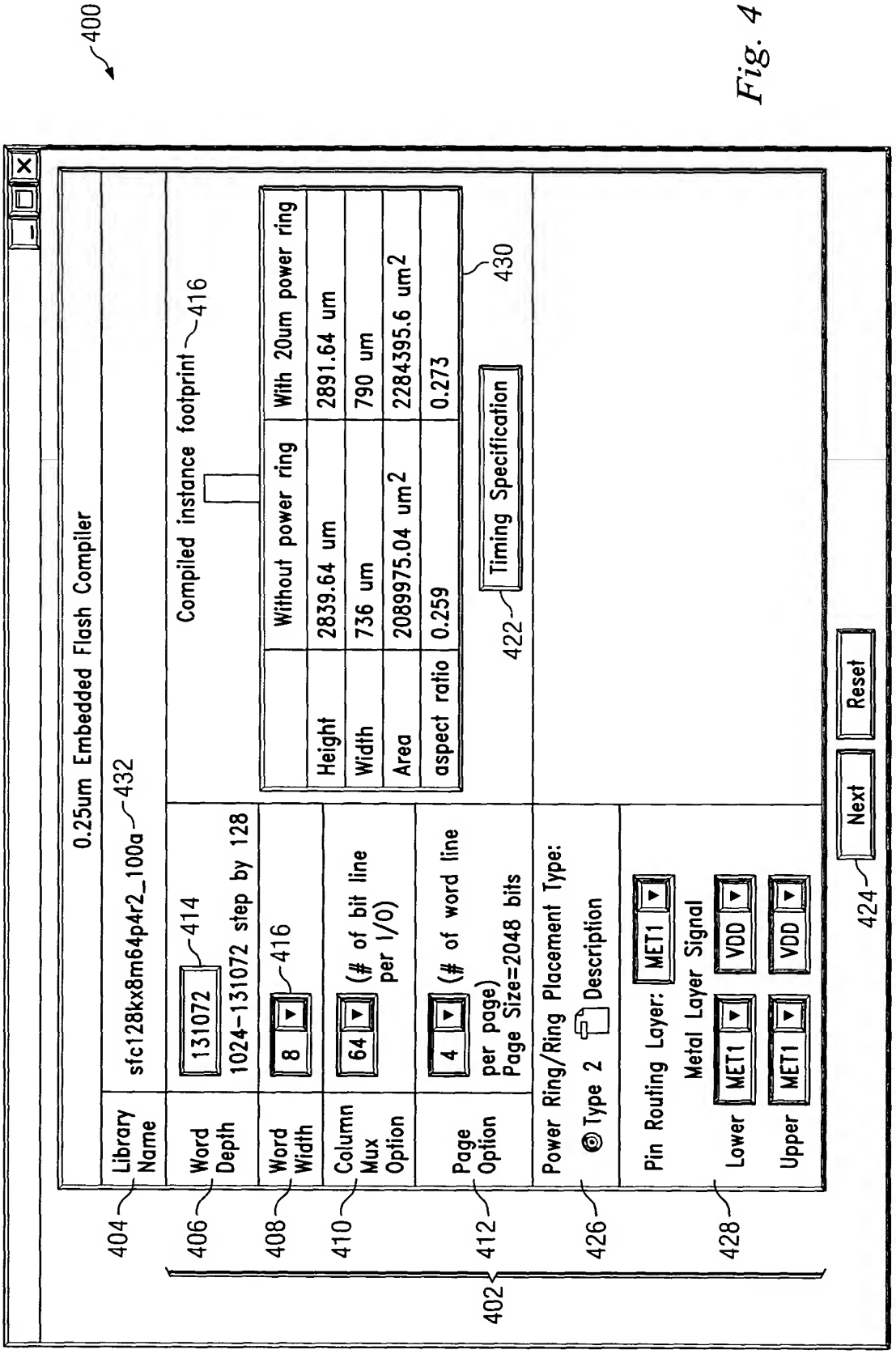

400
0.25um Embedded Flash Compiler
Library Name
sfc128kx8m64p4r2_100a
432
Word Depth
131072
414
1024–131072 step by 128
Word Width
8
416
Column Mux Option
64
(# of bit line per I/O)
Page Option
4
(# of word line per page)
Page Size=2048 bits
Power Ring/Ring Placement Type:
Type 2
Description
Pin Routing Layer:
MET1
Metal Layer Signal
Lower
MET1
VDD
Upper
MET1
VDD
Compiled instance footprint
416
Without power ring
With 20um power ring
Height
2839.64 um
2891.64 um
Width
736 um
790 um
Area
2089975.04 um2
2284395.6 um2
aspect ratio
0.259
0.273
Timing Specification
422
430
Next
Reset
424
402
404
406
408
410
412
426
428

Fig. 4

Fig. 5 4/12 500

Datasheet				
Library Name			sfc128kx8m64p4p4r2_100a	432
Word Depth			131072	
Word Width			8	
Column Mux Option			64	500a
Page Option			4	
Page Size			2048 bits	
Chip Height			2839.64 um	
Chip Width			736 um	
Area			2089975.04 um^2	
Aspect Ratio			0.259	
DC Electrical Characteristic(T_J=0°C to 125°C, V_{DD}=2.25V to 2.75V, V_{SS}=0V)				
Parameter	Symbol	Unit	Specification T_j=0~125°C	
Read operation current	IDD1	mA	8	500b
Program operation current		mA	7	
Erase current		mA	5	
Mass erase current		mA	5	
Static read current	IDD2	mA	5	
Standby current	ISB	uA	10	
Timing Parameters (T_J=0°C to +125°C, V_{DD}=2.25V to 2.75V, V_{SS}=0V, CLOAD=1pF) User mode				
Parameter	Symbol	Unit	Timing Numbers	
			Min	Max
X address access time	Txa	ns	–	50
Y address access line	Tya	ns	–	50
OE access time	Toa	ns	–	5
PROG/ERASE to NVSTR set up time	Tnvs	us	5	–
NVSTR hold time	Tnvh	us	5	–
NVSTR hold time (mass erase)	Tnvh1	us	100	–
NVSTR to program set up time	Tpgs	us	10	–
program hold time	Tpgh	ns	20	–
program time	Tprog	us	20	40
address/data set up time	Tads	ns	20	–
address/data hold time	Tadh	ns	20	–
recovery time	Trcv	us	1	–
Erase time	Terase	ms	20	–
Mass erase time	Tme	ms	200	–

500c

504 Add a new IP 506 Save as file Clean All DataSheet 508

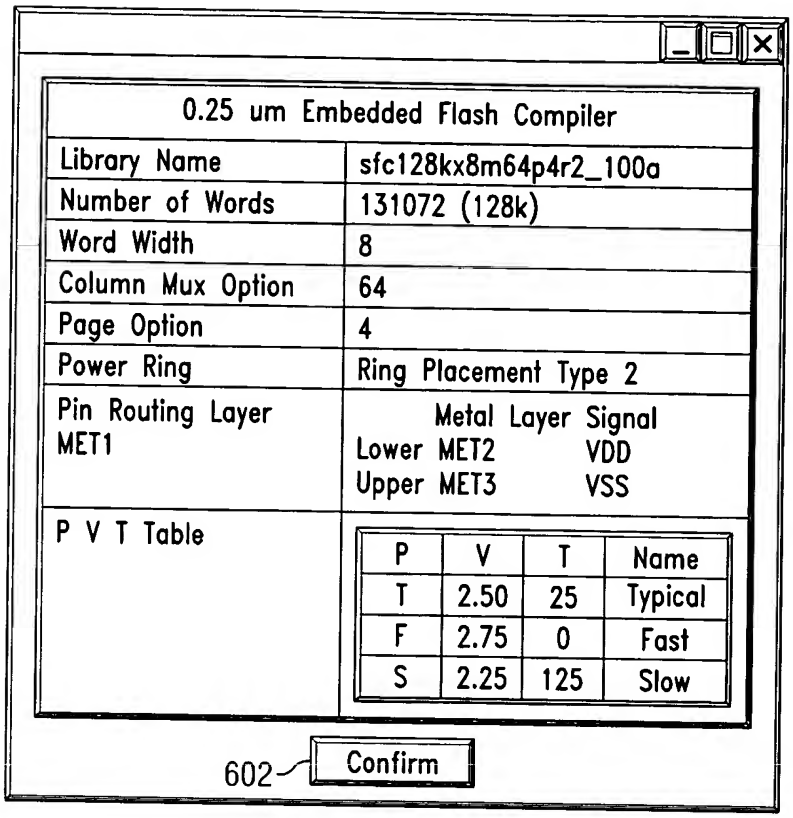

0.25 um Embedded Flash Compiler
Library Name
sfc128kx8m64p4r2_100a
Number of Words
131072 (128k)
Word Width
8
Column Mux Option
64
Page Option
4
Power Ring
Ring Placement Type 2
Pin Routing Layer
MET1
Metal Layer Signal
Lower MET2 VDD
Upper MET3 VSS
P V T Table
P V T Name
T 2.50 25 Typical
F 2.75 0 Fast
S 2.25 125 Slow
602
Confirm

Fig. 6

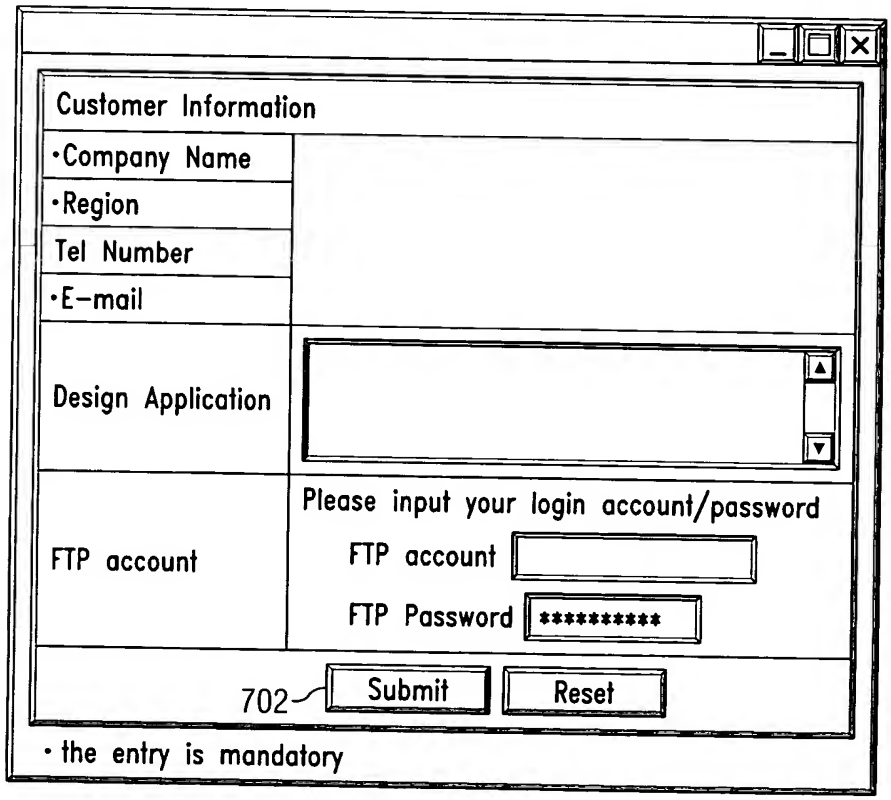

Customer Information
•Company Name
•Region
Tel Number
•E-mail
Design Application
FTP account
Please input your login account/password
FTP account
FTP Password
****
702
Submit
Reset
• the entry is mandatory
700

Fig. 7

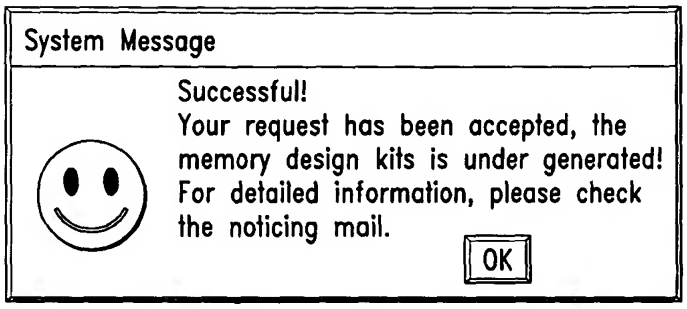


Fig. 8

Fig. 9

VIEWS	FILE EXTENSION	COMMENTS
CALIBRE NETLIST	.cali_cdl	NETLIST FOR CALIBRE LVS
HERCULES NETLIST	.herc_cdl	NETLIST FOR HERCULES LVS
LAYOUT	.gds	GDS FILE FOR FLASH INSTANCE
VERILOG	.v & .v_pg	VERILOG BEHAVIOR MODELS. .v DOESN'T HAVE THE LOCAL FLASH VDD AND AND VSS. .v_pg HAS THE LOCAL VDD AND VSS.
SYNOPSYS	.lib & .lib_pg	TIMING MODEL FOR SYNOPSYS. .lib DOESN'T HAVE THE LOCAL VDD AND VSS. .lib_pg HAS THE LOCAL VDD AND VSS.
APOLLO FRAME	.fram	APOLLO LAYOUT ABSTRACTION FOR ROUTABILITY. IT HAS SIZE, PIN LOCATION, BLOCKAGE INFORMATION. IT IS IN BINARY FORMAT.
APOLLO CELL	.cel	MILKYWAY FORMAT LAYOUT. IT HAS EVERYTHING EXCEPT IN DIFFERENT FILE FORMAT AS A gds FILE.
APOLLO TIMING	.tim	TIMING INFORMATION FOR APOLLO.
PHANTOM	.phantom_gds	TOP LEVEL LAYOUT INFORMATION. A PSUB TAB IS ADDED TO PASS THE LVS CHECK FROM THE APOLLO.
PHANTOM NETLIST	.phantom_cdl	TOP LEVEL NETLIST INFORMATION.
LIBRARY LEF (PHANTOM)	.lef	CADENCE LAYOUT ABSTRACTION FOR ROUTABILITY.
ANTENNA CLF	.antenna_clf	INPUT AND OUTPUT PINS GATE AREAS, SOURCE AND DRAIN AREA IN AVANT'S FORMAT.
ANTENNA LEF	.antenna_lef	INPUT AND OUTPUT PINS GATE AREAS, SOURCE AND DRAIN AREA IN CADENCE'S FORMAT.
DATA SHEET	.ds and .pdf	DOCUMENTATION FOR THE FLASH INSTANCE. .ds IS IN ASCII FORMAT WHILE .pdf IS IN pdf FORMAT. (.pdf FORMAT DATASHEET ISN'T AVAILABLE AT THIS MOMENT, IT WILL BE AVAILABLE WITH FUTURE RELEASE).

Fig. 10

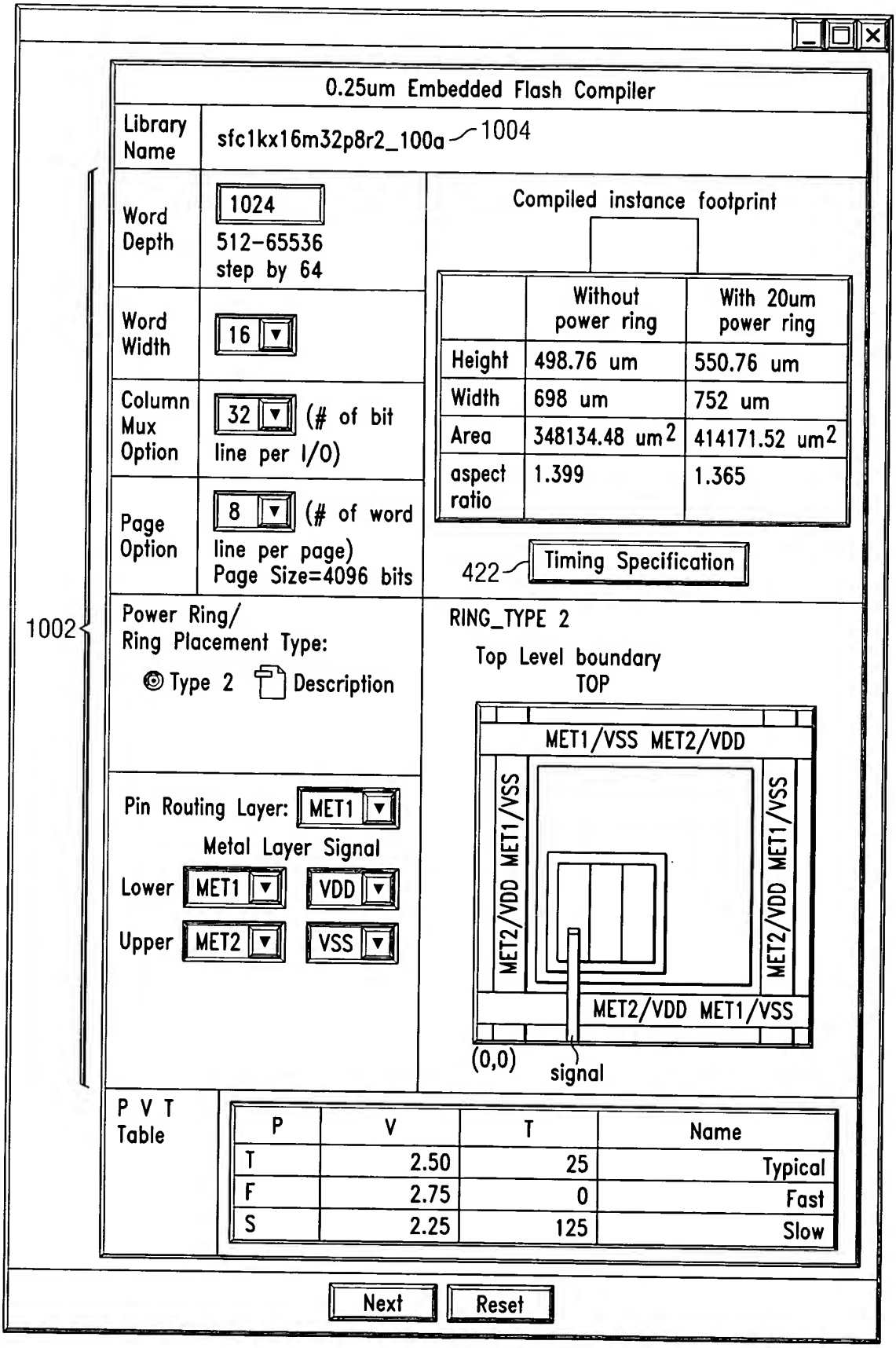

0.25um Embedded Flash Compiler
Library Name
sfc1kx16m32p8r2_100a
1004
Word Depth
1024
512–65536 step by 64
Word Width
16
Column Mux Option
32
(# of bit line per I/O)
Page Option
8
(# of word line per page)
Page Size=4096 bits
Compiled instance footprint
Without power ring
With 20um power ring
Height
498.76 um
550.76 um
Width
698 um
752 um
Area
348134.48 um2
414171.52 um2
aspect ratio
1.399
1.365
422
Timing Specification
1002
Power Ring/ Ring Placement Type:
Type 2
Description
RING_TYPE 2
Top Level boundary
TOP
MET1/VSS MET2/VDD
MET2/VDD MET1/VSS
MET2/VDD MET1/VSS
MET2/VDD MET1/VSS
(0,0)
signal
Pin Routing Layer:
MET1
Metal Layer Signal
Lower
MET1
VDD
Upper
MET2
VSS
P V T Table
P
V
T
Name
T
2.50
25
Typical
F
2.75
0
Fast
S
2.25
125
Slow
Next
Reset

Fig. 11 8/12 1100 1004

Combination Datasheet		
Library Name 432	sfc128kx8m64p4r2	sfc1kx16m32p8r2
Word Depth	131072	1024
Word Width	8	16
Column Mux Option	64	32
Page Option	4	8
Page Size	2048 bits	4096 bits
Chip Height	2839.64 um	498.76 um
Chip Width	736 um	698 um
Area	2089975.04 um^2	348134.48 um^2
Aspect Ratio	0.259	1.399

DC Electrical Characteristic(T_J=0°C to 125°C, V_{DD}=2.25V to 2.75V, V_{SS}=0V)

Parameter	Symbol	Unit	Specification T_j=0~125°C	Specification T_j=0~125°C
Read operation current	IDD1	mA	8	12
Program operation current		mA	7	7
Erase current		mA	5	5
Mass erase current		mA	5	5
Static read current	IDD2	mA	5	7
Standby current	ISB	uA	10	10

Timing Parameters (T_J=0°C to +125°C, V_{DD}=2.25V to 2.75V, V_{SS}=0V, CLOAD=1pF) User mode

Parameter	Symbol	Unit	Timing Numbers		Timing Numbers	
			Min	Max	Min	Max
X address access time	Txa	ns	–	50	–	20
Y address access line	Tya	ns	–	50	–	20
OE access time	Toa	ns	–	5	–	5
PROG/ERASE to NVSTR set up time	Tnvs	us	5	–	5	–
NVSTR hold time	Tnvh	us	5	–	5	–
NVSTR hold time (mass erase)	Tnvh1	us	100	–	100	–
NVSTR to program set up time	Tpgs	us	10	–	10	–
program hold time	Tpgh	ns	20	–	20	–
program time	Tprog	us	20	40	20	40
address/data set up time	Tads	ns	20	–	20	–
address/data hold time	Tadh	ns	20	–	20	–
recovery time	Trcv	us	1	–	1	–
Erase time	Terase	ms	20	–	20	–
Mass erase time	Tme	ms	200	–	200	–

Add a new IP | Save as Excel file | Clean All DataSheet

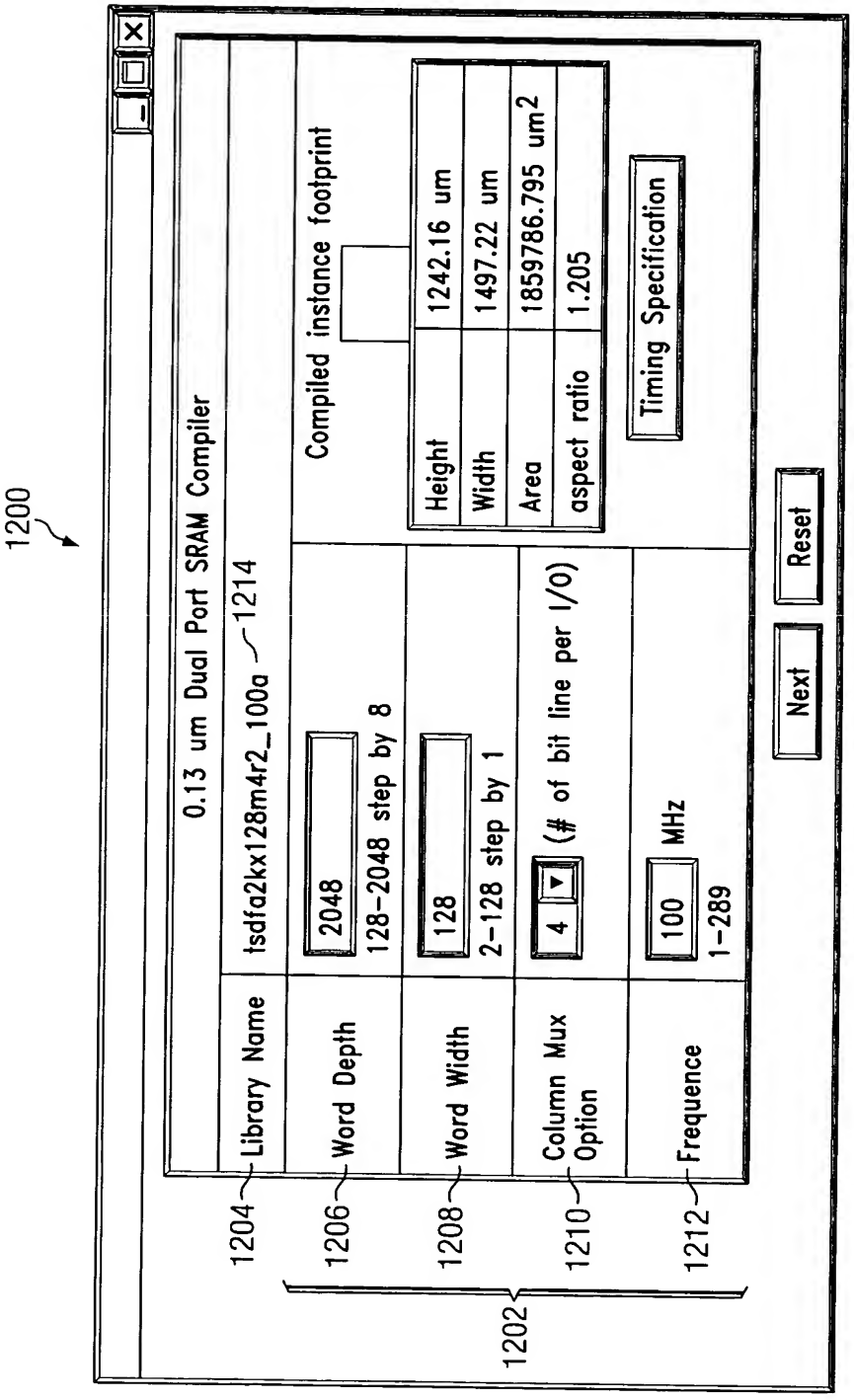

1200
0.13 um Dual Port SRAM Compiler
Library Name
tsdfa2kx128m4r2_100a
1214
Word Depth
2048
128–2048 step by 8
Word Width
128
2–128 step by 1
Column Mux Option
4
(# of bit line per I/O)
Frequence
100
MHz
1–289
1202
1204
1206
1208
1210
1212
Compiled instance footprint
Height
1242.16 um
Width
1497.22 um
Area
1859786.795 um2
aspect ratio
1.205
Timing Specification
Next
Reset

Fig. 12

Fig. 13A

1300

Datasheet				
Library Name 1214	tsdfa2kx128m4r2_100a			
Word Depth	2048			
Word Width	128			
Column Mux Option	4			
Power Ring Width	10.1 um			
Chip Height	1242.16 um			
Chip Width	1497.22 um			
Area	1859786.795 um^2			
Aspect Ratio	1.205			
Frequence	100 MHz			
DC Electrical Characteristic(T_J=0°C to 125°C, V_{DD}=1.35V to 1.65V, V_{SS}=0V)				
Parameter	Symbol	Fast process 1.65V, 0C	Typical process 1.5V, 25C	Slow process 1.35V, 125C
A-port cycle time (ns)	tcyca	3.465	4.97	8.421
B-port cycle time (ns)	tcycb	3.465	4.97	8.421
A-port access time (ns)	taa	3.394	4.861	8.185
B-port access time (ns)	tab	3.394	4.861	8.185
A-port address setup (ns)	tasa	0.261	0.26	0.486
B-port address setup (ns)	tasb	0.261	0.26	0.486
A-port address hold (ns)	taha	0	0	0.1
B-port address hold (ns)	tahb	0	0	0.1
A-port chip enable setup (ns)	tcsa	0.225	0.287	0.416
B-port chip enable setup (ns)	tcsb	0.225	0.287	0.416

TO Fig. 13B

FROM Fig. 13A

A-port chip enable hold (ns)	tcha	0	0	0
B-port chip enable hold (ns)	tchb	0	0	0
A-port write enable setup (ns)	twsa	0.153	0.196	0.273
B-port write enable setup (ns)	twsb	0.153	0.196	0.273
A-port write enable hold (ns)	twha	0	0	0
B-port write enable hold (ns)	twhb	0	0	0
A-port output enable (ns)	toea	0.498	0.654	1.091
B-port output enable (ns)	toeb	0.498	0.654	1.091
A-port output hi-z (ns)	toza	0.585	0.546	1.042
B-port output hi-z (ns)	tozb	0.585	0.546	1.042
A-port data setup (ns)	tdsa	0.213	0.262	0.261
B-port data setup (ns)	tdsb	0.213	0.262	0.261
A-port data hold (ns)	tdha	0	0	0
B-port data hold (ns)	tdhb	0	0	0
A-port clock high (ns)	tckha	0.3	0.393	0.447
B-port clock high (ns)	tckhb	0.3	0.393	0.447
A-port clock low (ns)	tckla	0.382	0.42	0.489
B-port clock low (ns)	tcklb	0.382	0.42	0.489
A & B port clock collision (ns)	tcc	0.791	1.069	1.642
Output load factor	Kload	0.166	0.215	0.236
AC current mA/port-MHz		0.321	0.282	0.246
Read AC current mA/port-MHz		0.303	0.263	0.221
Write AC current mA/port-MHz		0.34	0.302	0.272
Standby current uA		10.133	11.898	37.812

Add a new IP | Save as Excel file | Clean All DataSheet

Fig. 13B

1300

VIEWS	FILE EXTENSION	COMMENTS
LVS NETLIST	.spi	NETLIST FOR LVS
LAYOUT	.gds	GDS FILE FOR FLASH INSTANCE
VERILOG	.v	.V: VERILOG BEHAVIOR MODELS DOESN'T HAVE THE LOCAL VDD AND VSS.
SYNOPSYS	.lib & .lib_pg	.lib: TIMING MODEL FOR SYNOPSYS DOESN'T HAVE THE LOCAL VDD AND VSS. .lib_pg: HAS THE LOCAL VDD AND VSS.
APOLLO FRAME	.fram	APOLLO ABSTRACT VIEW FOR ROUTABILITY. IT CONTAINS SIZE, PIN LOCATIONS, AND BLOCKAGE INFORMATION IN BINARY FORMAT.
APOLLO CELL	.cel	LAYOUT INFORMATION IN MILKYWAY FORMAT. IT CONTAINS THE SAME INFORMATION AS A gds FILE, BUT IN DIFFERENT FORMAT.
APOLLO TIMING	.tim	TIMING INFORMATION FOR APOLLO
1LIBRARY LEF (PHANTOM)	.lef	CADENCE ABSTRACT VIEW FOR ROUTABILITY
ANTENNA CLF	.antenna_clf	INPUT AND OUTPUT PINS GATE AREAS, SOURCE AND DRAIN AREA IN AVANT'S FORMAT.
ANTENNA LEF	.antenna_lef	INPUT AND OUTPUT PINS GATE AREAS, SOURCE AND DRAIN AREA IN CADENCE'S FORMAT.
DATA SHEET	.ds and .pdf	DATASHEET IN ASCII FORMAT.

Fig. 14